Amendments to the Drawings:

In Fig. 2, a line separating Bundle 0 and Bundle 1 is misaligned. A corrected drawing of Fig. 2, having been amended to show the correct alignment of the line, is attached hereto in Appendix A.

REMARKS and ARGUMENTS

Claims 1-21 are pending in the Application. Claims 1, 2, 4, 5, 8-12, and 14-21 stand rejected. Claims 3, 6, 7 and 13 stand objected to as being based on a rejected claim but would be allowable if rewritten in independent form.

Allowable claims

Applicants appreciate the indication of allowability regarding Claims 3, 6, 7 and 13. Claims 3, 6 and 13 have been re-written in independent form, and therefore stand allowable. Claim 7, which depends from re-written Claim 6, also stands allowable.

Claim Rejections -35 USC § 112, 2nd paragraph

The Office Action rejects claims 8-10 because it asserts that the work "capable" is indefinite. Claims 8 – 10 have been amended to remove this word from the claims; the rejection has been overcome. Because no other rejection was made of Claims 8 – 10 in the Office Action, they stand allowable as amended, except that they depend from rejected base claims (Claim 5, which depends from Claim 1). Thus, Claims 8, 9 and 10 have been re-written in independent form to incorporate the limitations of Claims 1 and 5 as originally presented. Claims 8, 9 and 10 as amended herein should therefore be allowed to issue.

The Office Action also rejects Claims 14-15 because their use of the term "x" is in conflict with Claim 11, from which they depend. Applicants appreciate the Examiner's attention to detail and agree that the claims were confusing as originally presented. The claims have been amended to clarify that the number of non-NOP instructions is indicated by "n-x". The rejection has been overcome. Because no other rejection was made of Claims 14 and 15 in the Office Action, they stand allowable as amended, except that they depend from a rejected base claim

(Claim 11). Claim 14 has been amended to incorporate the limitations of Claim 11 as originally presented, rending the claim allowable. Claim 15, which depends from Claim 14, is also rendered allowable by such amendment. Claims 14 and 15 as amended herein should therefore be allowed to issue because all rejections have been overcome.

Claim Rejections -35 USC § 102(b)

The Office Action has rejected Claims 1-2, 4-5, and 11-12 under 35 U.S.C. § 102(b) as being anticipated by U.S. Pat. No. 5,893,143 to Tanaka et al. ("Tanaka"). However, the Office Action has failed to make a prima facie case of anticipation for the amended claims, and such rejections should be withdrawn.

"[F]or anticipation under 35 U.S.C. 102, the reference must teach *every aspect* of the claimed invention ..." MPEP 706.02 (emphasis added). "The identical invention must be shown *in as complete detail as contained in the ... claim.*" *Richardson v., Suzuki Motor Co.*, 868 F. 2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989) (emphasis added). Tanaka simply fails to disclose every aspect of the claimed invention. The Examiner has therefore failed to meet his burden of making a prima facie case of anticipation.

Tanaka pertains to a system for reducing the number of NOP operations stored in memory by a compiler. Main storage outside the processor stores instructions to be executed by the processor. (Tanaka, Col. 5, lines 9 – 16). The compiler deletes NOPs from the instructions stored in the memory. (Tanaka, Col. 5, lines 55 – 62). A compressed instruction string is instead stored in the memory. (*Id.*) When the instruction string is executed by the processor, mask information in the string allows the NOP to be inserted into the instruction field again. (Tanaka, Col. 6, lines 1 – 2).

Claim 1 recites, in part, "folding logic circuit to place, responsive to a NOP in the bundle, a "present" value in the NOP indicator field." Claim 16 recites, in part:

> folding logic circuit to allocate a buffer entry for one of the instructions, wherein the buffer entry includes a NOP indicator field;
>
> the folding logic circuit to place a "present" value in the NOP indicator field responsive to the presence of a NOP instruction in the bundle

The Office Action claims that these limitations are met by the compiler of Tanaka. However, Applicants disclose that their folding logic is ***processor*** logic that operates on instruction bundles that have been fetched from an instruction cache 102. They state that "[t]he processor 100 includes an instruction storage area 102, such as an L1 cache, for storing instructions" and that "[t]he processor 100 also includes a fetch engine 104 to fetch instructions from the storage area 102." (Application, para. 14) One of skill in the art will recognize that this processor-internal processing occurs after compilation has occurred and that the cache 102 includes binary instructions that have already been compiled or assembled. In contrast to Tanaka, Applicants disclose that NOP instructions may be stored in the instruction storage area 102 (see NOP Instruction (indicator) in Fig. 1).

Applicants disclose at paragraph 17 that "for at least one embodiment folding logic 116 is implemented as part of a decoder." Also, Applicants disclose that the folding logic is part of a processor: "Referring to Fig. 5, processing system 500 includes a memory system 502 and a processor 504 that includes folding logic 116 and a buffer 210 of the format shown in Fig. 2." (Application, para. 50). Clearly, the folding logic 116 is a hardware circuit. It is shown in Fig. 5 as being part of the processor 504, not as being part of the instruction 510 in memory 502, which is where a compiler would reside. Claims 1 and 16 have been amended to make this distinction more clear. The Office Action thus fails to make a prima facie case of

anticipation for Claims 1 and 16, as amended. Claims 1 and 16 are therefore allowable for at least these reasons. In addition, Claims 2, 4, and 5, which depend from Claim 1, are also allowable for at least these reasons. Claims 17 – 21, which depend from Claim 16, are also allowable for at least these reasons.

Claim 11 has also been amended to make it clear that the processing of claim 11 occurs during execution of a bundle of instructions, not during pre-compilation processing such as that discussed in Tanaka. Claim 11 is therefore allowable as amended and the rejection should be withdrawn. Claim 12, which depends from Claim 11, is also allowable for at least this reason.

Claim Rejections -35 USC § 103(a)

The Office Action has rejected Claims 16 - 21 under 35 U.S.C. § 103(a) as being unpatentable over Tanaka in view of Boyd et al (Patent No. 5,895,487). However, the Office Action has failed to make a prima facie case of obviousness for the claims, and such rejections should be withdrawn.

The legal requirements for a prima facie case of obviousness are clear. The prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991) (MPEP 2144). The Office Action has not met these requirements.

The prior art references cited by the Office Action do not either alone or in combination disclose, teach or suggest all the claim limitations of Claims 16 - 21. Neither reference teaches the following limitations of Claim 16:

folding logic circuit to allocate a buffer entry for one of the instructions, wherein the buffer entry includes a NOP indicator field;

the folding logic circuit to place a "present" value in the NOP indicator field responsive to the presence of a NOP instruction in the bundle.

The Office Action relies on its rejections of 1-2, 4-5 and 11-12 to similarly reject Claims 16, except that the Office Action relies on Boyd to show a DRAM. However, Applicants have discussed above that Tanaka does not shows a hardware folding logic circuit of a processor. Neither does Boyd. Because neither the Tanaka nor Boyd reference teaches all of the recited elements of Claim 16, their combination is similarly fruitless for making a prima facie case of obviousness. Thus, all claims remaining in the case are allowable.

Accordingly, Applicants respectfully submit that the applicable rejections have been overcome and must all be withdrawn. Applicants reserve all rights with respect to the application of the doctrine equivalents. Applicant respectfully requests that a timely Notice of Allowance be issued in this case. If the Examiner feels that an interview would help to resolve any remaining issues in the case, the Examiner is invited to contact Shireen Bacon of Intel, at (512) 732-3917.

Please charge any shortages and credit any overcharges to our Deposit Account No. 02-2666.

Respectfully submitted,

Dated: February 17, 2006

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APPENDIX A

Amended Figure for Fig. 2